Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (**currently amended**) A method for reducing poly-depletion in a dual gate CMOS fabrication process, comprising the steps of:

forming an STI oxide film ~~at proper sites of a silicon substrate~~ **adjacent an active region** having an NMOS forming region and a PMOS forming region **in a silicon substrate,**

wherein the area above the boundary between the active region and the STI oxide film is referred to as the fringing portion,

wherein the height of the STI oxide film not at or near the fringing portion (referred to as a non-fringing portion) is higher than the height of the STI oxide film at or near the fringing portion and the height of the active region;

sequentially forming a gate dielectric film and a polysilicon film on the ~~silicon substrate including~~ the STI oxide film **and the active region formed on the silicon substrate**

wherein the polysilicon film formed at or near the fringing portion is thicker than the non-fringing portion of the polysilicon film;

selectively implanting an N-type impurity and a P-type impurity into the portions of the polysilicon film, which correspond respectively to the NMOS

forming region and PMOS forming region of the silicon substrate, by ion implantation; and

patterning the polysilicon film having the selectively ion-implanted N-type and P-type impurities and the gate dielectric film to form an N+ polysilicon gate in the NMOS region of the silicon substrate and a P+ polysilicon gate in the PMOS region of the silicon substrate,

wherein the ion implantation of the N-type impurity is performed by implanting phosphorus in a dose of 1 to 2 x $10^{16}/cm^2$,

after the step of patterning the polysilicon film, heating at a temperature higher than 800 degree Celsius allowing thermal diffusion of the ion-implanted impurities into the bottom portion of the polysilicon film formed at the boundary between the active region and the STI oxide film.

2. **(cancelled)**

3. (original) The method according to claim 1, wherein said polysilicon film has a thickness ranging from 1900 to 2100 Å.

4. **(cancelled)**

5. (withdrawn) A method for reducing poly-depletion in a dual gate CMOS fabrication process, comprising the steps of:

forming an STI oxide film at proper sites of a silicon substrate having an NMOS forming region and a PMOS forming region;

sequentially forming a gate dielectric film and a polysilicon film on the silicon substrate including the STI oxide film;

selectively implanting an N-type impurity and a P-type impurity into the portions of the polysilicon film, which correspond respectively to the NMOS forming region and PMOS forming region of the silicon substrate, by ion implantation; and

patterning the polysilicon film having the selectively ion-implanted N-type and P-type impurities and the gate dielectric film to form an N+ polysilicon gate in the NMOS region of the silicon substrate and a P+ polysilicon gate in the PMOS region of the silicon substrate, wherein the polysilicon film has a thickness ranging from 1600 to 1800 Å.

6. (withdrawn) A method for reducing poly-depletion in a dual gate CMOS fabrication process, comprising the steps of:

forming an STI oxide film at proper sites of a silicon substrate having an NMOS forming region and a PMOS forming region;

sequentially forming a gate dielectric film and a polysilicon film on the silicon substrate including the STI oxide film;

selectively implanting an N-type impurity and a P-type impurity into the portions of the polysilicon film, which correspond respectively to the NMOS

forming region and PMOS forming region of the silicon substrate, by ion implantation; and

patterning the polysilicon film having the selectively ion-implanted N-type and P-type impurities and the gate dielectric film to form an N+ polysilicon gate in the NMOS region of the silicon substrate and a P+ polysilicon gate in the PMOS region of the silicon substrate, wherein the height of the STI oxide film measured at the top of the silicon substrate is less or equal to 0.

7. (withdrawn) The method according to claim 6, wherein the height of said STI oxide film is adjusted by increasing a target polishing amount of CMP when forming the STI oxide film or by wet etching the surface of the STI oxide film after formation of the film.

8. (withdrawn) A method for reducing poly-depletion in a dual gate CMOS fabrication process, comprising the steps of:

forming an STI oxide film at proper sites of a silicon substrate having an NMOS forming region and a PMOS forming region;

sequentially forming a gate dielectric film and a polysilicon film on the silicon substrate including the STI oxide film;

selectively implanting an N-type impurity and a P-type impurity into the portions of the polysilicon film, which correspond respectively to the NMOS forming region and PMOS forming region of the silicon substrate, by ion implantation; and

patterning the polysilicon film having the selectively ion-implanted N-type and P-type impurities and the gate dielectric film to form an N+ polysilicon gate in the NMOS region of the silicon substrate and a P+ polysilicon gate in the PMOS region of the silicon substrate, wherein the formation of the polysilicon film and the ion-implantation of the impurities are repeated at least twice.

9. (withdrawn) The method according to claim 8, wherein said polysilicon film has a final thickness ranging from 1900 to 2100 Å.

10. (withdrawn) The method according to claim 9, wherein said final thickness of the polysilicon film is identical to the sum of the thicknesses obtained in every repeated polysilicon film formation.